ABSTRACT

A scalable flash EEPROM cell having a semiconductor substrate with a drain and a source and a channel therebetween. A select gate is positioned over a portion of the channel and is insulated therefrom. A floating gate is a spacer having a bottom surface positioned over a second portion of the channel and is insulated therefrom. The floating gate has two side surfaces extending from the bottom surface. A control gate is over the floating gate and includes a first portion that is adjacent the floating gate first side surface, and a second portion adjacent the floating gate second side surface.